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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,003	12/10/2003	Choon-Yul Oh	50869/DBP/Y35	9397

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PASADENA, CA 91109-7068

EXAMINER
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NGUYEN, KIMNHUNG T

ART UNIT	PAPER NUMBER
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2629

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/734,003

Applicant(s)

OH, CHOON-YUL

Examiner

Kimnhung Nguyen

Art Unit

2629

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 21 December 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-16 is/are allowed.
- 6) ☒ Claim(s) 17 is/are rejected.
- 7) ☒ Claim(s) 18-22 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

This Application has been examined. The claims 1-22 are pending. The examination results are as following.

#### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jinno (US 2002/0167472) in view of Chung et al. (US 2004/0051685).

As to claim 17, Jinno discloses in fig. 1, a display device comprising a display element for displaying a portion of an image in response to a current being applied; a transistor (Tr1) having a main electrode coupled to a voltage source (PVdd); a first capacitor (C1) for charging a first voltage Vsc; and a first switch, coupled between the transistor (Tr1) and the display for intercepting a current supplied to the display element from the transistor (Tr1).

However, Jinno does not disclose the first voltage corresponding to a threshold voltage of the transistor.

Chung et al. discloses in fig. 3, an active matrix organic light emitting diode comprising the voltage corresponding to a threshold voltage of the transistor (see abstract, see 0024).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the voltage corresponding to a threshold voltage of the transistor as taught by Chung et al. in to the display system of Jinno having the first voltage for producing the claimed invention because this would provide to the threshold voltage compensation circuit block, and then the video signal is input to the gate of the driving transistor of pixels. As a result, the threshold voltage nonuniformity between pixels can be reduced. Therefore, also, high-quality, large-sized displays can be implemented without increasing the area occupied by transistor in the pixels (see 0013).

*Allowable Subject Matter*

3. Claims 1-16 are allowed.
4. Claims 18-22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

None of the cited art teaches or suggests that a luminescent display comprising a second capacitor coupled between the power supply line and the second transistor for storing a voltages corresponding to the data signal; and a second switch for electrically isolating a second main electro of the first transistor from the luminescent element during voltage-charging of the first capacitor in response to a control signal, the first transistor supplying a current corresponding to the sum of the voltage charged in the first and second capacitors as claim 1; or a third transistor having a control electrode thereof coupled to a previous scan line for a pixel that was previously scanned, and coupled between the power supply line and the first and second capacitors; and a

fourth transistor having a control electrode thereof coupled to the previous scan line, and being coupled between the second capacitor and the second main electrode of the first transistor, the first transistor supplying a current corresponding to a voltage charged in the first and second capacitors as claim 7; or applying a selection signal for selecting the pixel coupled to the scan line; and receiving the data voltage from the data line in response to the selection signal, and supplying a current corresponding to the sum of the compensated gate voltage and the data voltage to the luminescent element as claim 13; or wherein a first voltage is charged in the first capacitor during a first period, and a second voltage is charged in a second capacitor during a second period as claim 18.

### ***Response To Arguments***

5. Applicant's arguments filed on 12/21/06 have been considered but they are not persuasive.

Applicant states that "there is no motivation to combine Jinno and Chung references in a manner to meet the claim requirement. First, the two references are individually complete. In Jinno's FIG. 1, "a voltage value of the data voltage signal is held in the storage capacitor C. The conducting state (resistance) between the source (S) and the drain (D) of the second transistor Tr2 is controlled by the amount of charge held in the storage capacitor C. Further, the OEL element is driven by the current value which is determined by the power source voltage PVdd and the controlled resistance. More specifically, the resistance value of the second transistor Tr2, and thus the current value applied to the OEL, is controlled by the data voltage signal input to the first transistor Tr1. Therefore, the capacitor C is used to control the

Art Unit: 2629

resistance between the source (S) and the drain D of the second transistor Tr2 and has nothing to do with the threshold voltage of the transistor Tr2”.

Examiner respectfully disagrees because Jinno discloses in fig. 1, a transistor (Tr1) having a main electrode coupled to a voltage source (PVdd); a first capacitor (C1) for charging a first voltage Vsc; and a switch, coupled between the transistor (Tr1) and the display for intercepting a current supplied to the display element from the transistor (Tr1). However, Jinno does not disclose the first voltage corresponding to a threshold voltage of the transistor. Chung et al. discloses in fig. 3, an active matrix organic light emitting diode comprising the voltage corresponding to a threshold voltage of the transistor (see abstract, see 0024). Therefore, the combination of the Jinno and Chung et al. references are satisfied for its intended purpose. For these reasons, these rejection are maintained.

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

*Correspondence*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kimnhung Nguyen whose telephone number is (571) 272-7698. The examiner can normally be reached on MON-FRI, FROM 8:30 AM-5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kimnhung Nguyen  
Patent Examiner  
February 21, 2007



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